Synthesizer Decade (623-2080-001, -002, -003, -004)

Rockwell International

instructions

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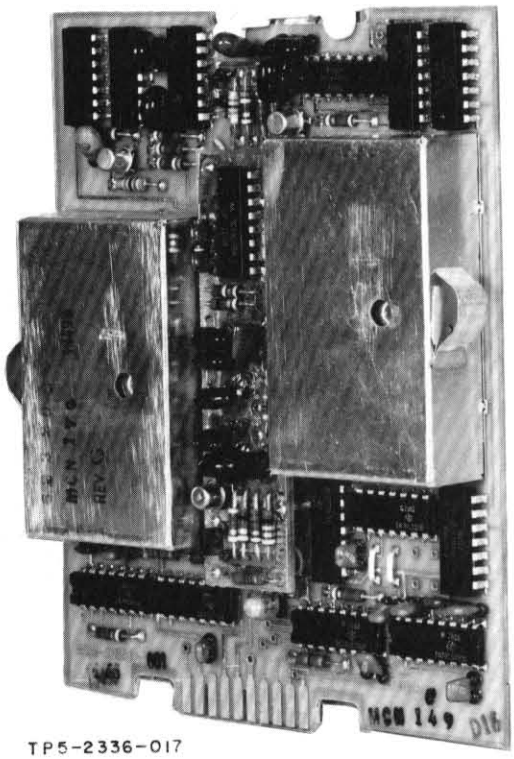
1. DESCRIPTION.

Synthesizer Decades 623-2080-001, -002, -003, -004, shown in figure 1 and listed in table 1, are 2-layer planar cards with 20-pin edge-on connectors (2 layers, 10 pins each). The modules differ only in strapping and frequency control/output, as indicated on the schematic, figure 14.

Table 1. Cards Covered by These Instructions.

CARD TYPE	COLLINS PART NO
100-kHz synthesizer decade	623-2080-001
10-kHz synthesizer decade	623-2080-002
1-kHz synthesizer decade	623-2080-003
100/10-Hz synthesizer decade	623-2080-004

The synthesizer decade module consists of translator logic, translator vco, output mixer, output logic, output vco, low-pass filter circuits, a divide-by-10 output circuit, and a loss-of-lock (LOL) monitor circuit.



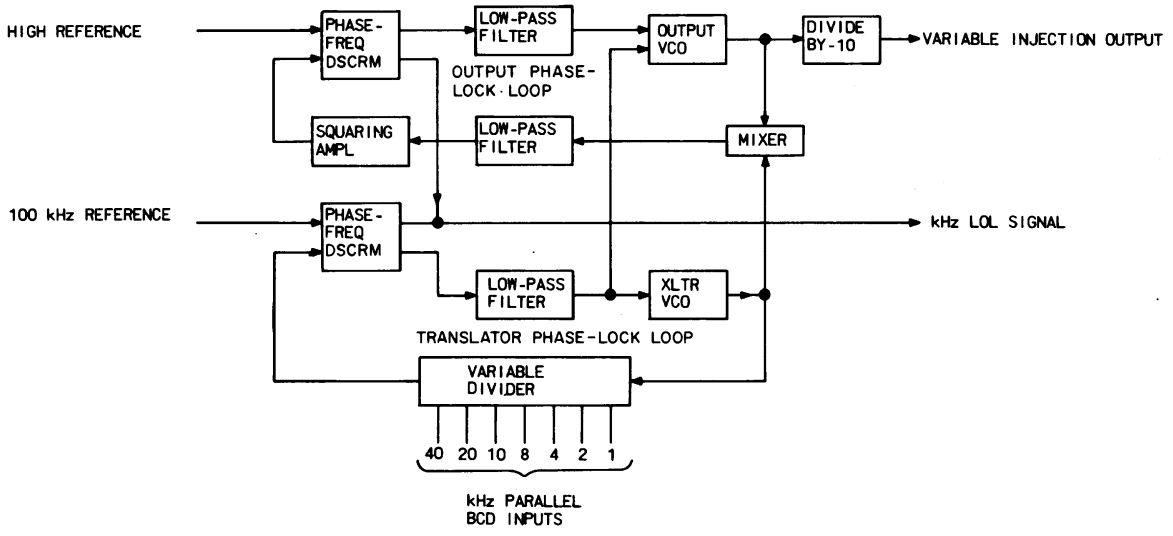
Synthesizer Decade
Figure 1

2. PRINCIPLES OF OPERATION

2.1 General (Refer to figure 2.)

The synthesizer decade module receives bcd frequency control signals, a 100-kHz reference signal, and a high-reference signal, and generates a variable injection signal output and a lock signal output (logic 1 for lock). The variable injection signal output is used as the high-reference signal in the next frequency step in the generation of a 79.35001- to 109.35-MHz variable injection signal output.

The translator logic circuits receive a 100-kHz reference input, a translator vco signal, and a bcd frequency input. The bcd frequency input is used to



Synthesizer Decade, Block Diagram
Figure 2

program a variable frequency divider (division ratio depends on strapping and bcd inputs). The programmed variable frequency divider output (100 kHz) and the 100-kHz reference input are supplied to a phase/frequency discriminator that provides a control voltage proportional to the phase/frequency difference between its inputs.

The translator vco circuit receives the control voltage signal from the translator logic circuits and is driven to and phase-locked at the variable frequency as programmed by the variable divider bcd inputs to the translator logic circuits. The translator vco output is supplied to the translator logic circuits for clocking and lock signal generation. The translator vco output is supplied to the output mixer circuits for frequency mixing.

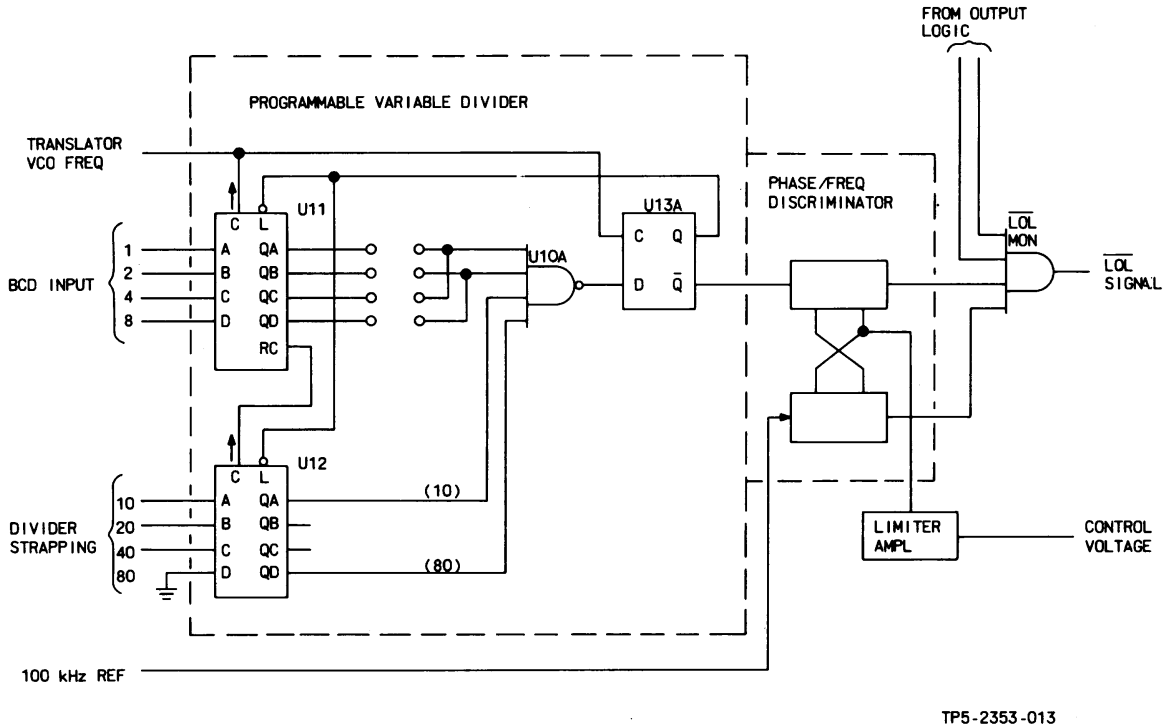
The output mixer circuit receives the translator signal input and the output vco signal input, mixes them, and supplies a reference input to the phase/frequency discriminator. In the phase/frequency discriminator the mixer reference input is compared with the high-reference input and produces an output control voltage.

The output vco circuit receives the output control voltage signal from the output logic circuits and the translator tracking voltage from the translator vco circuits. The translator tracking voltage provides a reference voltage for the output vco, and the output control voltage drives the output vco until it is locked at the variable injection frequency. The output vco output is supplied to a fixed divide-by-10 output circuit. The fixed divide-by-10 circuit output is supplied as a reference to the following decade or output module.

2.2 Translator Logic Circuits

The translator logic circuits receive a 100-kHz reference input, a translator vco signal output, and bcd frequency inputs, and supplies a control voltage output signal to the translator vco.

Refer to figure 3. The translator vco signal output (table 2) is supplied as the clock input to a programmable variable divider. The output of the programmable variable divider (100 kHz) is supplied to a phase/frequency discriminator and is compared with a 100-kHz reference input. A phase or frequency difference in the discriminator causes a control voltage input increase or decrease to adjust the frequency of the vco. If there is no phase or frequency difference, the discriminator provides a logic 1 lock signal output indicating the vco frequency is locked.



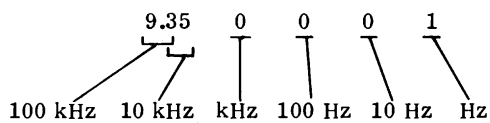
Translator Logic Circuits
Figure 3

Table 2. Decade Versus VCO Inputs/Outputs.

DECADE	TRANSLATOR VCO FREQ (MHz)	HIGH REF INPUT FREQ TO OUTPUT VCO (MHz)	OUTPUT VCO FREQ BEFORE DIVIDER (MHz)
100 kHz	9.5 to 8.6	0.85 to 0.750001	10.35 to 9.350001
10 kHz	7.8 to 6.9	0.70 to 0.60001	8.50 to 7.50001
1 kHz	6.4 to 5.5	0.60 to 0.5001	7.00 to 6.0001
100 Hz	5.4 to 4.5	0.60 to 0.501	6.00 to 5.001
10 Hz	5.4 to 4.5	0.60 to 0.51	6.00 to 5.01

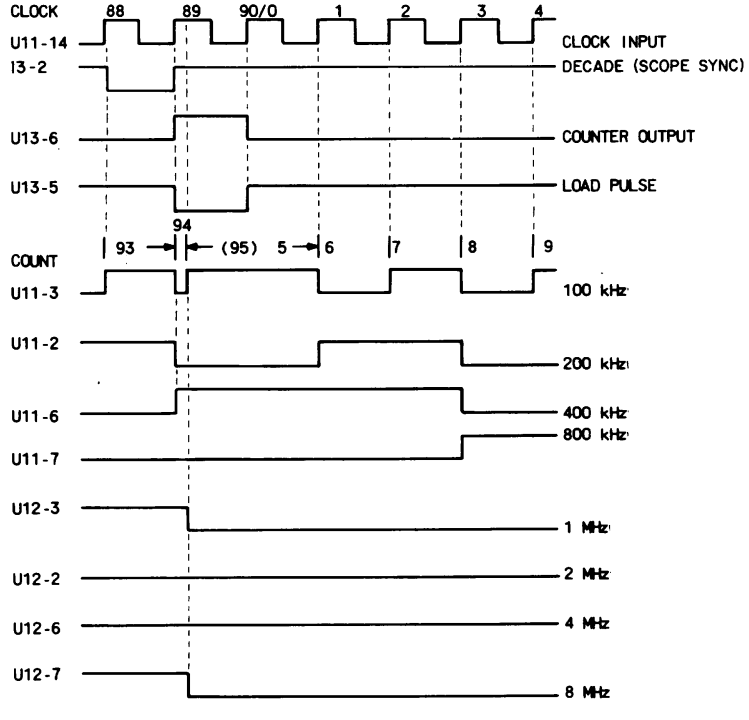
Note

The above high-reference inputs are shown as they would be in a 1-Hz tuned synthesizer. In a 10-Hz tuned synthesizer, there would be no 10-Hz decade and the 100-Hz high-reference input would be 0.60 to 0.51 MHz, the 1-kHz high-reference input would be 0.60 to 0.501 MHz, etc. In a 100-Hz tuned synthesizer, there would be no 100-Hz decade and the 1-kHz high reference would be 0.60 to 0.51 MHz, the 10-kHz high reference would be 0.70 to 0.601 MHz, etc. Output vco frequency at 100-kHz output has the following tuning characteristics.



The programmable variable divider is programmed by the bcd frequency inputs. Refer to table 3. For example, if a bcd input of 0 is applied, the up/down decade counter is programmed to load the count 0 at any time a load signal (logic 0) is applied. This programs the variable divider to count from 0 (first count 1) to 95 (last count 95/0). This causes the output of the variable divider to be 1/95th of the clock input or a divide-by-95 with a bcd input of 0. Note that, as the bcd input goes up 1, 2, 3, etc, the division ratio goes down -94, -93, -92, etc. Also note that, for the divide-by circuit to operate as a constant, the last count 95 also must be the loaded count (in the case of bcd 0, count 0). To do this, prerecognition of count 95 is required. Look-ahead circuit of U10A performs this function. At clock 93 (count 93), gate U10A is ANDed and supplies a logic 0 input to U13A-D. With a logic 0 at U13A-D, clock 94 (count 94) causes U13A-$\overline{Q}$ to go to logic 0 and loads decade counter to bcd input (ANDed output U10A is removed). At clock 94, U13A-Q supplies a pulse to the phase/frequency discriminator. Clock 95 (count 00) causes U13A-Q to go to logic 1 and enables decade counter to count on the next clock. Next clock is one above the bcd programmed input. Note that count 94 initiates the output from the divider and count 95 appears only as the bcd programmed input. Refer to figure 4. A 500-kHz programmed input is shown; the same principles apply to any other programmed bcd input.

The preceding discussion pertained to the 100-kHz decade card. Differences between the cards can be seen in figures 5 through 8 and tables 3 through 6. Note that the internal strapping changes and the external input divider strapping changes cause a change in the programmable variable divider.



PROGRAMMED BCD INPUTS		
100 kHz	PIN NO.	LOGIC LEVEL
1	U11-15	1
2	U11-1	0
4	U11-10	1
8	U11-9	0
10	U12-15	FXD 0
20	U12-1	FXD 0
40	U12-10	FXD 0
80	U12-9	FXD 0

NOTE:
EXAMPLE SHOWN IS FOR 500 kHz.

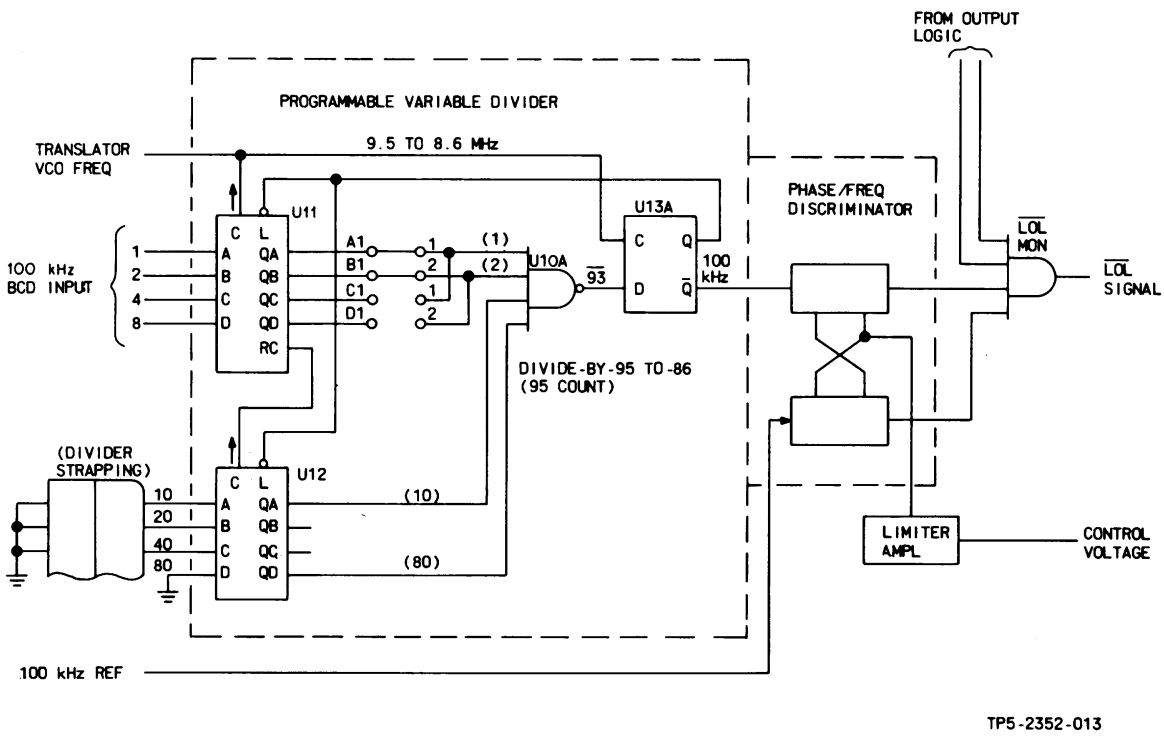
TP5-2365-013

Variable Divider, Inputs and Outputs
Figure 4

Table 3. 100-kHz Decade, Logic Truth Table.

BCD INPUT (100 kHz)	DIVIDER INPUTS								OUTPUT COUNT	DIVIDE-BY	LOOP FREQ (MHz)
	U11				U12						
	A	B	C	D	**A	**B	**C	*D			
0	0	0	0	0	0	0	0	0	0	95	9.5
1	1	0	0	0	0	0	0	0	1	94	9.4
2	0	1	0	0	0	0	0	0	2	93	9.3
3	1	1	0	0	0	0	0	0	3	92	9.2
4	0	0	1	0	0	0	0	0	4	91	9.1
5	1	0	1	0	0	0	0	0	5	90	9.0
6	0	1	1	0	0	0	0	0	6	89	8.9
7	1	1	1	0	0	0	0	0	7	88	8.8
8	0	0	0	1	0	0	0	0	8	87	8.7
9	1	0	0	1	0	0	0	0	9	86	8.6

*Internally strapped for logic 0 (ground).
**Externally strapped for logic 0 (ground) at pins 7, 16, and 17.

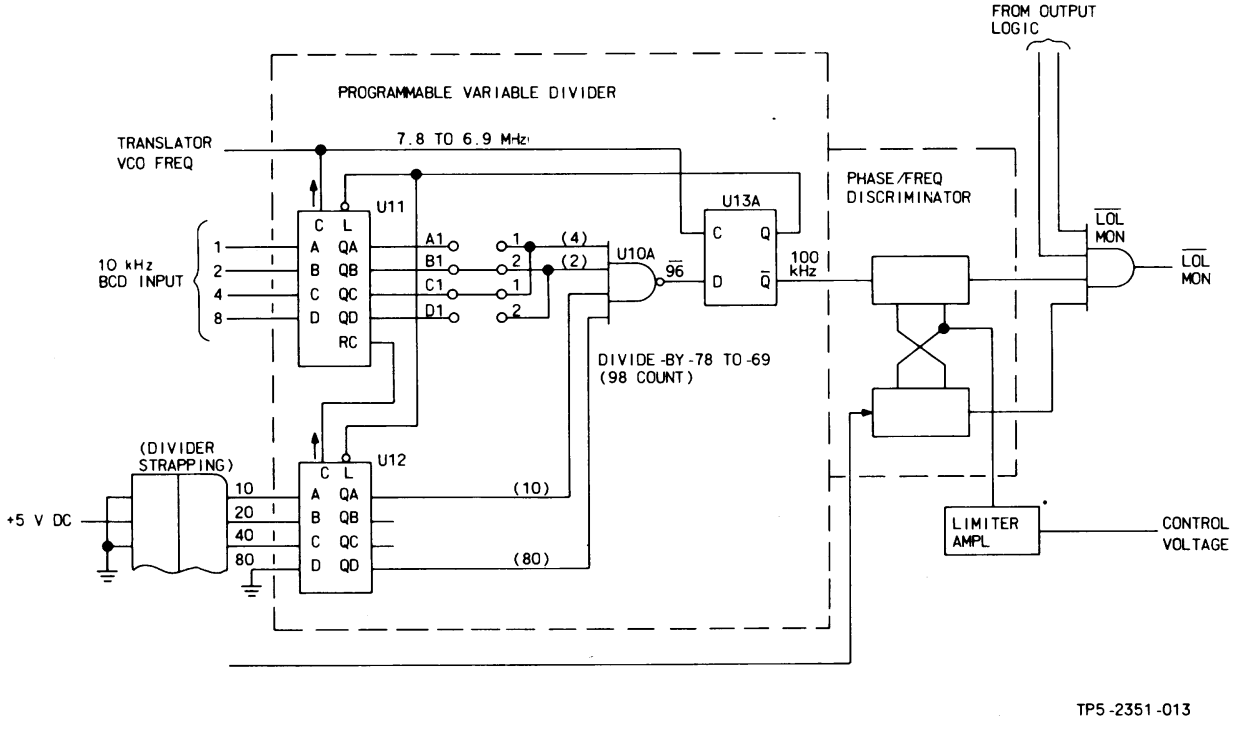


100-kHz Decade Translator, Logic Circuit
Figure 5

Table 4. 10-kHz Decade, Logic Truth Table.

BCD INPUT (10 kHz)	DIVIDER INPUTS								OUTPUT COUNT	DIVIDE-BY	LOOP FREQ (MHz)
	U11				U12						
	A	B	C	D	**A	[1]B	**C	*D			
0	0	0	0	0	0	1	0	0	20	78	7.8
1	1	0	0	0	0	1	0	0	21	77	7.7
2	0	1	0	0	0	1	0	0	22	76	7.6
3	1	1	0	0	0	1	0	0	23	75	7.5
4	0	0	1	0	0	1	0	0	24	74	7.4
5	1	0	1	0	0	1	0	0	25	73	7.3
6	0	1	1	0	0	1	0	0	26	72	7.2
7	1	1	1	0	0	1	0	0	27	71	7.1
8	0	0	0	1	0	1	0	0	28	70	7.0
9	1	0	0	1	0	1	0	0	29	69	6.9

*Internally strapped for logic 0 (ground).
**Externally strapped for logic 0 (ground) at pins 7 and 16.
[1]Externally strapped for logic 1 (+5.2 V dc) at pin 17.

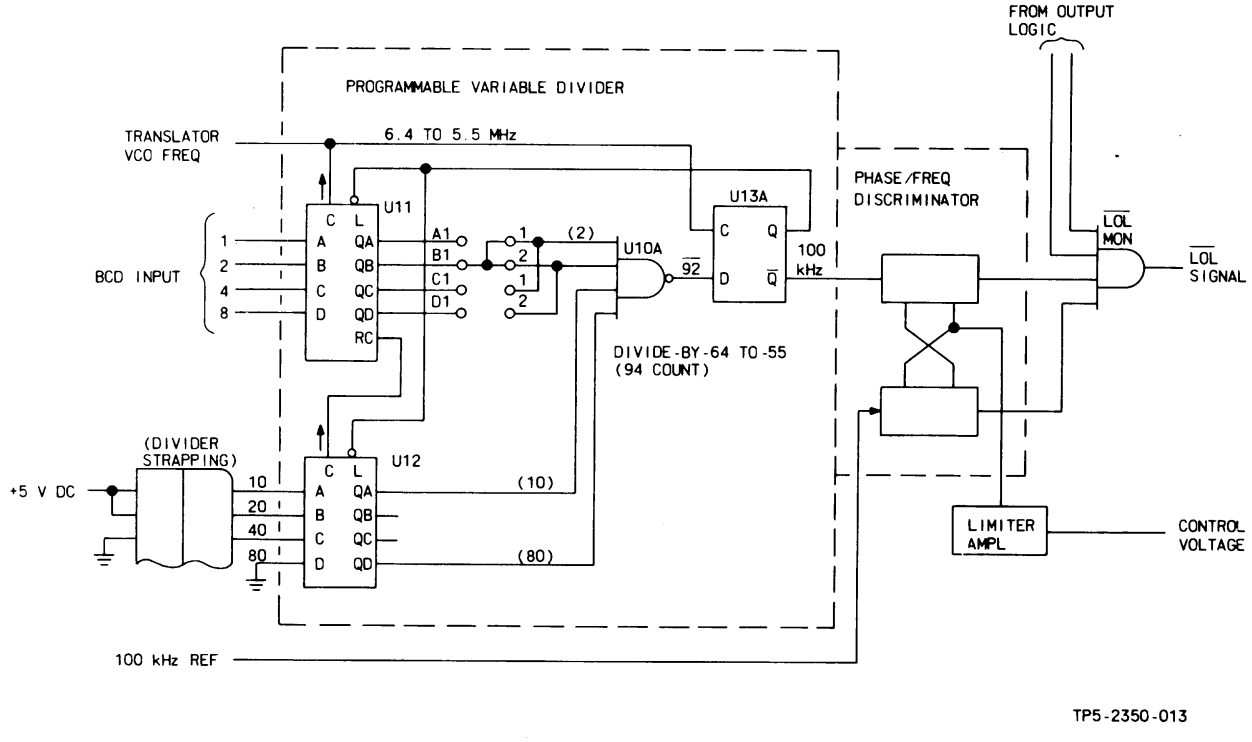


10-kHz Decade Translator, Logic Circuit
Figure 6

Table 5. 1-kHz Decade, Logic Truth Table.

BCD INPUT (1 kHz)	DIVIDER INPUTS								OUTPUT COUNT	DIVIDE-BY	LOOP FREQ (MHz)
	U11				U12						
	A	B	C	D	[1]A	[1]B	**C	*D			
0	0	0	0	0	1	1	0	0	30	64	6.4
1	1	0	0	0	1	1	0	0	31	63	6.3
2	0	1	0	0	1	1	0	0	32	62	6.2
3	1	1	0	0	1	1	0	0	33	61	6.1
4	0	0	1	0	1	1	0	0	34	60	6.0
5	1	0	1	0	1	1	0	0	35	59	5.9
6	0	1	1	0	1	1	0	0	36	58	5.8
7	1	1	1	0	1	1	0	0	37	57	5.7
8	0	0	0	1	1	1	0	0	38	56	5.6
9	1	0	0	1	1	1	0	0	39	55	5.5

*Internally strapped for logic 0 (ground).
**Externally strapped for logic 0 (ground) at pin 16.
[1]Externally strapped for logic 1 (+5.2 V dc) at pins 7 and 17.

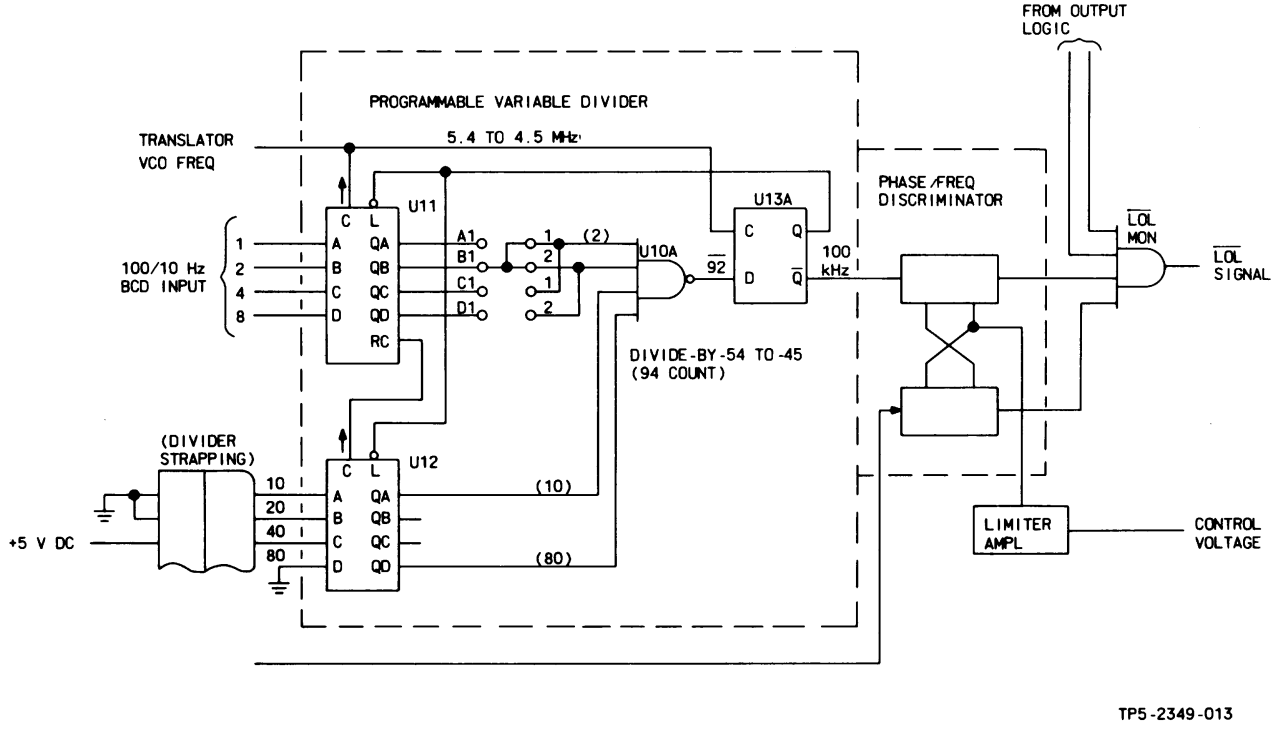


1-kHz Decade Translator, Logic Circuit
Figure 7

Table 6. 100/10-Hz Decade, Logic Truth Table.

BCD INPUT (100/10 Hz)	DIVIDER INPUTS								OUTPUT COUNT	DIVIDE-BY	LOOP FREQ (MHz)
	U11				U12						
	A	B	C	D	**A	**B	[1]C	*D			
0	0	0	0	0	0	0	1	0	40	54	5.4
1	1	0	0	0	0	0	1	0	41	53	5.3
2	0	1	0	0	0	0	1	0	42	52	5.2
3	1	1	0	0	0	0	1	0	43	51	5.1
4	0	0	1	0	0	0	1	0	44	50	5.0
5	1	0	1	0	0	0	1	0	45	49	4.9
6	0	1	1	0	0	0	1	0	46	48	4.8
7	1	1	1	0	0	0	1	0	47	47	4.7
8	0	0	0	1	0	0	1	0	48	46	4.6
9	1	0	0	1	0	0	1	0	49	45	4.5

*Internally strapped for logic 0 (ground).
**Externally strapped for logic 0 (ground) at pins 7 and 17.
[1]Externally strapped for logic 1 (+5.2 V dc) at pin 16.



100/10-Hz Decade Translator, Logic Circuit
Figure 8

2.3 Translator VCO Circuits

The translator vco circuits receive a control voltage from the translator logic circuits. The control voltage drives the vco to the required translator frequency. The translator signal output is supplied through one buffer amplifier to the output mixer circuits and the translator logic circuits.

2.4 Output Mixer Circuits

The output mixer circuits receive a translator signal input (table 2) from the translator vco. The translator vco signal is mixed with the output vco frequency (table 2) and a resulting difference frequency (table 2, same as high-reference input) is supplied to the output logic circuits.

2.5 Output Logic Circuits

The output logic circuits receive the output mixer difference frequency and a high-reference input signal (table 2), and supply a control voltage output signal to operate the output vco.

Refer to figure 9. The output mixer difference frequency is supplied through a squaring amplifier to a phase/frequency discriminator. This frequency is compared with the high-reference input signal. A phase or frequency difference in the discriminator causes the control voltage to increase or decrease to adjust the frequency of the vco. If there is no phase or frequency difference, the discriminator provides a logic 1 lock signal output and the vco frequency locks.

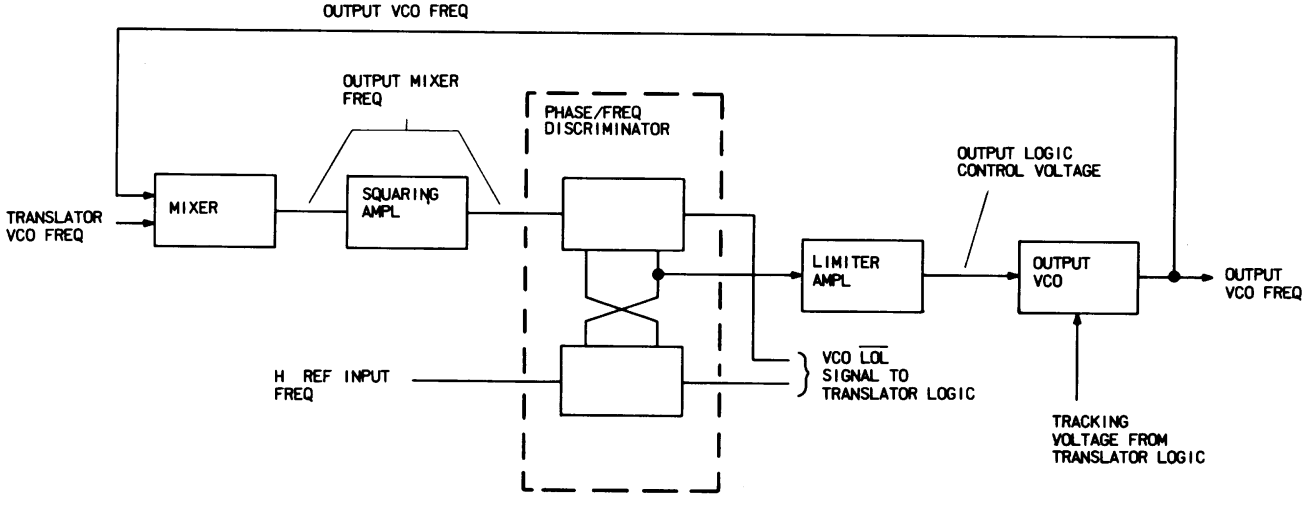
2.6 Output VCO Circuits

The output vco circuits receive a control voltage from the output logic circuits and a tracking voltage from the translator logic circuits. The tracking voltage from the translator logic circuits provides a reference for the output vco, and the control voltage from the output logic circuits drives the output vco to the required output vco frequency. The output vco frequency is supplied through a fixed divide-by-10 circuit and provides a reference frequency to the unit under control for additional frequency mixing and generation. Note that the tracking voltage from the translator logic circuits is used as a reference for the output vco, thus summing the translator frequency information and the output vco frequency information.

2.7 Up/Down Decade Counter 74LS190 (Refer to table 7.)

The 74LS190 up/down decade counter is a 4-bit decade counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when input conditions are met.

A high at the enable input inhibits counting. A LOC at the enable input and a low-to-high clock transition triggers the four master/slave flip-flops. The enable input should be changed only when the clock is high. The down/up input determines the direction of the count. When low, the count goes up; when high, the count goes down.



Output Logic Circuits
Figure 9

Table 7. Up/Down Decade Counter, Logic Truth Table.

PROGRAMMABLE INPUTS				COUNT	BCD OUTPUTS			
A	B	C	D		QA	QB	QC	QD
0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	0	0
0	1	0	0	2	0	1	0	0
1	1	0	0	3	1	1	0	0
0	0	1	0	4	0	0	1	0
1	0	1	0	5	1	0	1	0
0	1	1	0	6	0	1	1	0
1	1	1	0	7	1	1	1	0
0	0	0	1	8	0	0	0	1
1	0	0	1	9	1	0	0	1

E (enable): logic 0 enables counter; logic 1 inhibits counter.

L (load): logic 0 programs the bcd output count to be set at the bcd count of the programmable inputs; the next clock pulse counts one higher/lower (up/down).

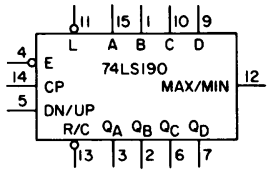
DU (down/up): logic 0 counts up; logic 1 counts down.

CP (clock pulse): logic 0-to-logic 1 transition advances counter.

RC (ripple clock): logic 0 pulse equal to 1/2 clock cycle when an overflow occurs.

MM (maximum/minimum count): logic 1 pulse equal to full clock cycle when an overflow or underflow occurs.

These counters are programmable. The outputs may be preset to any state by placing a low on the load input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the state of the clock input. This allows the counters to be used as modulo-N dividers by modifying the count length with the preset inputs.



Up/Down Decade Counter 74LS190
Figure 10

Two outputs are available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters are cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

2.8 Decade Counter 74LS90 (Refer to table 8.)

The 74LS90 decade counter is a high-speed, monolithic decade counter consisting of four dual-rack, master-slave flip-flops internally interconnected to provide a divide-by-2 counter and a divide-by-5 counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logical 0 or to a binary coded decimal (bcd) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes.

a. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the bcd count sequence in table 8. In addition to a conventional 0 reset, inputs are provided to reset a bcd 9 count for nine's complement decimal applications.
b. If a symmetrical divide-by-10 count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of 10, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-10 square wave is obtained at output A.
c. For operation as a divide-by-2 counter and divide-by-5 counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-2 function. The BD input is used to obtain binary divide-by-5 operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

Table 8. Decade Counter 74LS90, Logic Truth Table.

*BCD COUNT SEQUENCE				
COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

**RESET/COUNT							
RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	Count			
0	X	0	X	Count			
0	X	X	0	Count			
X	0	0	X	Count			

*Output A connected to input BD for BCD count.
**X indicates that either a logical 1 or a logical 0 may be present.

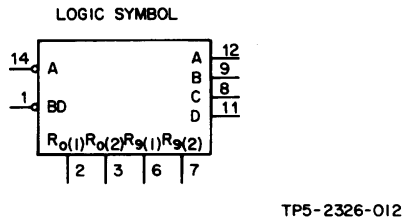
2.9 Dual D-Type Flip-Flop With Preset and Clear 74LS74 (Refer to table 9.)

The 74LS74 consists of dual high-speed D-type flip-flops. Information on the D input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either high or low level, the D-input signal has no effect.

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

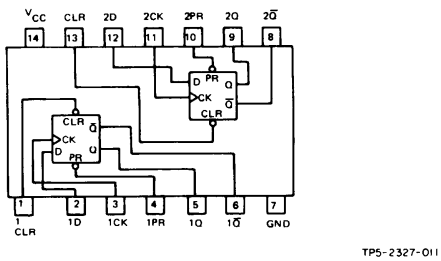
Test equipment and power sources required to test, troubleshoot, and repair the synthesizer decade are listed in the maintenance section of this instruction book.



Decade Counter 74LS90
Figure 11

3.2 Testing

The test procedures in table 10 check total performance of the synthesizer decade. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.



Dual D-Type Flip-Flop With Preset and Clear 74LS74
Figure 12

Table 9. Dual D-Type Flip-Flop With Preset and Clear 74LS74, Logic Truth Table.

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	*H	*H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of the unit containing the synthesizer decade that is to be tested.		
	b. Remove cover from the synthesizer section of the unit.		
	c. Remove synthesizer decade and install it on an extender card and place it in the unit.		
	d. Set unit LINE SELECTOR switch to 115 V.		
	e. Connect unit to 115-V ac power source and set power on.		
	f. Measure dc voltage from P1-20 and P1-2 to P1-6 (ground).	+5.2 ±0.2 V dc.	Check unit synthesizer voltage regulator.
	g. Measure dc voltage from P1-10 to P1-6 (ground).	NLT +19.5 V dc, NMT +20.8 V dc.	Check unit synthesizer voltage regulator.
2. 100-kHz decade 623-2080-001	***Note*** CR1, CR2, CR3, and CR4 are located under metal can shields. These shields must be in place during testing and adjustments. Refer to figure 13 for test point locations on the rear of the synthesizer decade.		
	a. Using a frequency counter, measure the high reference input between P1-14 and P1-4 (ground).	800 ±50 kHz. Note actual frequency.	Check unit 10-kHz decade.
	b. Set FREQUENCY KHZ control on front panel to 09900.00 (or 09900.0).		
	c. Measure the dc voltage at the cathode end of CR3-CR4. (Refer to note and chart at end of test 2 for voltages and output frequencies at different 100-kHz settings.)	10.0 ±0.1 V dc.	Adjust L9 for 10.0 ±0.1 V dc. If L9 adjustment does not correct the problem, check Q4, Q5, and associated circuit.
(Cont)	d. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	940 ±5 kHz. (Actual should equal 935 kHz plus one-tenth of the difference between 850 kHz and the actual frequency in step a.)	Adjust L7 for actual frequency required with 1.5 V dc at anode end of CR1-CR2. If L7 adjustment does not correct the problem, check Q1, Q2, and associated circuits.

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	e. Measure the dc voltage at the anode end of CR1-CR2.	1.5 ±0.5 V dc.	Same as step d.
	f. Note the dc voltage at the anode end of the anode end of CR1-CR2 while moving the 100-kHz frequency control from 9 down to 0.	NLT 1.0 V dc and NMT 2.0 V dc at any frequency control setting.	Adjust L7 so that all settings fall into the 1.0- to 2.0-V dc reading.
	g. Set FREQUENCY KHZ control on front panel to 09000.00 (or 09000.0).		
	h. Using a frequency counter, measure the high reference input between P1-14 and P1-4 (ground).	850 ±0.5 kHz.	Check unit 10-kHz decade.
	i. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	1035 ±0.5 kHz.	Check U11, U12, U13, and associated circuits.
	j. Set FREQUENCY KHZ control on front panel to 09900.00 (or 09900.0).		
	k. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	945 ±0.5 kHz.	Check U11, U12, U13, and associated circuits.
	l. Measure the dc voltage at P1-12 to ground.	NLT +3.5 V dc. **Note** RCV FAULT, EXCTR FAULT, or R/E FAULT indicator lighting indicates that result of step m is satisfactory.	Check U3, U8, U9, and U10.
	m. Ground P1-5 while noting the voltage at P1-12.	NMT 0.5 V dc.	Check U6, U7, U8, U9, and U10.
	n. Remove P1-5 ground.		
	o. Set front-panel PWR switch off.		
	p. Remove 10-kHz decade from unit under test.		
	q. Set front-panel PWR switch on.		
	r. Measure the dc voltage at P1-12 to ground.	NMT 0.5 V dc.	Check U1, U2,U3, and U10.
(Cont)	s. Set front-panel PWR switch off.		

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>2. (Cont)</td><td>t. Replace 10-kHz decade in unit under test.

Note

The following chart is shown with an input frequency of 850 ±5 kHz. The actual output frequency with any input frequency can be determined using the following formula.

$AF = LF - 10\ kHz + \frac{850\ kHz - IF}{10}$

AF = actual output frequency at P1-1.

LF = output frequency listed in chart for associated 100-kHz frequency digit.

IF = actual input frequency.

<table>
<tr><th>100-kHz FREQ DIGIT</th><th>CR3-CR4 DC VOLTAGE</th><th>FREQ OUTPUT P1-1 (kHz)</th></tr>
<tr><td>9</td><td>10.00 ±0.1</td><td>945 ±0.5</td></tr>
<tr><td>8</td><td>*10.30</td><td>955 ±0.5</td></tr>
<tr><td>7</td><td>*10.55</td><td>965 ±0.5</td></tr>
<tr><td>6</td><td>*10.85</td><td>975 ±0.5</td></tr>
<tr><td>5</td><td>*11.15</td><td>985 ±0.5</td></tr>
<tr><td>4</td><td>*11.40</td><td>995 ±0.5</td></tr>
<tr><td>3</td><td>*11.70</td><td>1005 ±0.5</td></tr>
<tr><td>2</td><td>*11.95</td><td>1015 ±0.5</td></tr>
<tr><td>1</td><td>*12.25</td><td>1025 ±0.5</td></tr>
<tr><td>0</td><td>*12.50</td><td>1035 ±0.5</td></tr>
</table>
Note

Table shown with an input frequency of 850 ±5 kHz [front-panel FREQUENCY KHZ setting of 09X00.00 (or 09X00.0)].

*Reference voltage only. Voltages will vary from board to board.</td><td></td><td></td></tr>
<tr><td>3. 10-kHz decade 623-2080-002

(Cont)</td><td>Note

CR1, CR2, CR3, and CR4 are located under metal can shields. These shields must be in place during testing and adjustments. Refer to figure 13 for test point locations on the rear of the synthesizer decade.

a. Using a frequency counter, measure the high reference input between P1-14 and P1-4 (ground).

b. Set FREQUENCY KHZ control on front panel to 09990.00 (or 09990.0).</td><td>650 ±50 kHz. Note actual frequency.</td><td>Check unit 1-kHz decade.</td></tr>
</table>

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	c. Measure the dc voltage at the cathode end of CR3-CR4 (refer to note and chart at end of test 3 for voltages and output frequencies at different 10-kHz settings).	10.45 ±0.1 V dc.	Adjust L9 for 10.00 ±0.1 V dc. If L9 adjustment does not correct the problem, check Q4, Q5, and associated circuit.
	d. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	755 ±5 kHz. (Actual should equal 750 kHz plus one-tenth of the difference between 700 kHz and the actual frequency in step a.)	Adjust L7 for actual frequency required with 1.5 V dc at anode end of CR1-CR2. If L7 adjustment does not correct the problem, check Q1, Q2, and associated circuits.
	e. Measure the dc voltage at the anode end of CR1-CR2.	1.5 ±0.5 V dc.	Same as step d.
	f. Note the dc voltage of the anode end of CR1-CR2 while moving the 10-kHz frequency control from 9 down to 0.	NLT 1.0 V dc and NMT 2.0 V dc at any frequency control setting.	Adjust L7 so that all settings fall into the 1.0- to 2.0-V dc reading.
	g. Set FREQUENCY KHZ control on front panel to 09900.00 (or 09900.0).		
	h. Using a frequency counter, measure the high reference input between P1-14 and P1-4 (ground).	700 ±0.5 kHz.	Check unit 1-kHz decade.
	i. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	850 ±0.5 kHz.	Check U11, U12, U13, and associated circuits.
	j. Set FREQUENCY KHZ control on front panel to 09990.00 (or 09990.0).		
	k. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	760 ±0.5 kHz.	Check U11, U12, U13, and associated circuits.
	l. Measure the dc voltage at P1-12 to ground.	NLT +3.5 V dc. ***Note*** RCV FAULT, EXCTR FAULT, or R/E FAULT indicator lighting indicates that result of step m is satisfactory.	Check U3, U8, U9, and U10.
(Cont)	m. Ground P1-5 while noting the voltage at P1-12.	NMT 0.5 V dc.	Check U6, U7, U8, U9, and U10.

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	n. Remove P1-5 ground.		
	o. Set front-panel PWR switch off.		
	p. Remove 1-kHz decade from unit under test.		
	q. Set front-panel PWR switch on.		
	r. Measure the dc voltage at P1-12 to ground.	NMT 0.5 V dc.	Check U1, U2, U3, and U10.
	s. Set front-panel PWR switch off.		
	t. Replace 1-KHZ decade in unit under test.		

Note

The following chart is shown with an input frequency of 700 ±5 kHz. The actual output frequency with any input frequency can be determined using the following formula.

$$AF = LF - 10\ kHz + \frac{700\ kHz - IF}{10}.$$

AF = actual output frequency at P1-1.

LF = output frequency listed in chart for associated 10-kHz frequency digit.

IF = actual input frequency.

10-kHz FREQ DIGIT	CR3-CR4 DC VOLTAGE	FREQ OUTPUT P1-1 (kHz)
9	10.00 ±0.1	760 ±0.5
8	*10.30	770 ±0.5
7	*10.55	780 ±0.5
6	*10.85	790 ±0.5
5	*11.10	800 ±0.5
4	*11.40	810 ±0.5
3	*11.75	820 ±0.5
2	*12.00	830 ±0.5
1	*12.35	840 ±0.5
0	*12.65	850 ±0.5

Note

Table shown with an input frequency of 700 ±5 kHz [front-panel FREQUENCY KHZ setting of 099X0.00 (or 099X0.0)].

*Reference voltage only. Voltages will vary from board to board.

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. 1-kHz decade 623-2080-003	**Note** CR1, CR2, CR3, and CR4 are located under metal can shields. These shields must be in place during testing and adjustments. Refer to figure 13 for test point locations on the rear of the synthesizer decade.		
	a. Using a frequency counter, measure the high reference input between P1-14 and P1-4 (ground).	550 ±50 kHz. Note actual frequency.	Check unit 100-kHz decade.
	b. Set FREQUENCY KHZ control on front panel to 09999.00 (or 09999.0).		
	c. Measure the dc voltage at the cathode end of CR3-CR4 (refer to note and chart at end of test 4 for voltages and output frequencies at different 1-kHz settings).	10.0 ±0.1 V dc.	Adjust L9 for 10.0 ±0.1 V dc. If L9 adjustment does not correct the problem, check Q4, Q5, and associated circuit.
	d. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	605 ±5 kHz. (Actual should equal 600 kHz plus one-tenth of the difference between 610 kHz and the actual frequency in step a.)	Adjust L7 for actual frequency required with 1.5 V dc at anode end of CR1-CR2. If L7 adjustment does not correct the problem, check Q1, Q2, and associated circuits.
	e. Measure the dc voltage at the anode end of CR1-CR2.	1.5 ±0.5 V dc.	Same as step d.
	f. Note the dc voltage at the anode end of CR1-CR2 while moving the 1-kHz frequency control from 9 down to 0.	NLT 1.0 V dc and NMT 2.0 V dc at any frequency control setting.	Adjust L7 so that all settings fall into the 1.0- to 2.0-V reading.
	g. Set FREQUENCY KHZ control on front panel to 09990.00 (or 09990.0).		
	h. Using a frequency counter, measure the high reference input between P1-14 and P1-4 (ground).	600 ±0.5 kHz.	Check unit 100-kHz decade.
	i. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	700 ±0.5 kHz.	Check U11, U12, U13, and associated circuits.
(Cont)	j. Set FREQUENCY KHZ control on front panel to 09999.00 (or 09999.0).		

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	k. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	610 ±0.5 kHz.	Check U11, U12, U13, and associated circuits.
	l. Measure the dc voltage at P1-12 to ground.	NLT +3.5 V dc.	Check U3, U8, U9, and U10.
		Note RCV FAULT, EXCTR FAULT, or R/E FAULT indicator lighting indicates that result of step m is satisfactory.	
	m. Ground P1-5 while noting the voltage at P1-12.	NMT 0.5 V dc.	Check U6, U7, U8, U9, and U10.
	n. Remove P1-5 ground.		
	o. Set front-panel PWR switch off.		
	p. Remove decade in 100-Hz slot (A18) from unit under test.		
	q. Set front-panel PWR switch on.		
	r. Measure the dc voltage at P1-12 to ground.	NMT 0.5 V dc.	Check U1, U2, U3, and U10.
	s. Set front-panel PWR switch off.		
	t. Replace decade in 100-Hz slot (A18) in unit under test.		
(Cont)	***Note*** The following chart is shown with an input frequency of 600 ±5 kHz. The actual output frequency with any input frequency can be determined using the following formula. $AF = LF - 10\ kHz + \frac{600\ kHz - IF}{10}$. AF = actual output frequency at P1-1. LF = output frequency listed in chart for associated 1-kHz frequency digit. IF = actual input frequency.		

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>4. (Cont)</td><td>
<table>
<tr><th>1-kHz FREQ DIGIT</th><th>CR3-CR4 DC VOLTAGE</th><th>FREQ OUTPUT P1-1 (kHz)</th></tr>
<tr><td>9</td><td>10.00 ±0.1</td><td>610 ±0.5</td></tr>
<tr><td>8</td><td>*10.40</td><td>620 ±0.5</td></tr>
<tr><td>7</td><td>*10.85</td><td>630 ±0.5</td></tr>
<tr><td>6</td><td>*11.25</td><td>640 ±0.5</td></tr>
<tr><td>5</td><td>*11.70</td><td>650 ±0.5</td></tr>
<tr><td>4</td><td>*12.10</td><td>660 ±0.5</td></tr>
<tr><td>3</td><td>*12.55</td><td>670 ±0.5</td></tr>
<tr><td>2</td><td>*12.95</td><td>680 ±0.5</td></tr>
<tr><td>1</td><td>*13.40</td><td>690 ±0.5</td></tr>
<tr><td>0</td><td>*13.80</td><td>700 ±0.5</td></tr>
</table>
Note
Table shown with an input frequency of 600 ±5 kHz [front-panel FREQUENCY KHZ setting of 0999X.00 (or 0999X.0)].

*Reference voltage only. Voltages will vary from board to board.
</td><td></td><td></td></tr>
<tr><td>5. 100/10-Hz decade 623-2080-004

(Cont)</td><td>Note
CR1, CR2, CR3, and CR4 are located under metal can shields. These shields must be in place during testing and adjustments. Refer to figure 13 for test-point locations on the rear of the synthesizer decade.

a. Using a frequency counter, measure the high reference input between P1-14 and P1-4 (ground).

b. If decade installed in 100-Hz slot (A18), set FREQUENCY KHZ control to 09999.90 (or 09999.9).

If decade installed in 10-Hz slot (A17), set FREQUENCY KHZ control to 09999.99.

c. Measure the dc voltage at the cathode end of CR3-CR4 (refer to note and chart at end of test 5 for voltages and output frequencies at different 100- or 10-Hz settings).</td><td>550 ±50 kHz. Note actual frequency.

9.5 ±0.1 V dc.</td><td>Check unit 10-Hz decade or end decade.

Adjust L9 for 9.5 ±0.1 V dc. If L9 adjustment does not correct the problem, check Q4, Q5, and associated circuit.</td></tr>
</table>

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	d. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	515 ±5 kHz. (Actual should equal 510 kHz plus one-tenth of the difference between 600 kHz and the actual frequency in step a.)	Adjust L7 for actual frequency required with 1.5 V dc at anode end of CR1-CR2. If L7 adjustment does not correct the problem, check Q1, Q2, and associated circuits.
	e. Measure the dc voltage at the anode end of CR1-CR2.	1.5 ±0.5 V dc.	Same as step d.
	f. Note the dc voltage at the anode end of CR1-CR2 while moving the 100- or 10-Hz frequency control from 9 down to 0 (Change 100-Hz control if installed as 100-Hz decade or 10-Hz control if installed as 10-Hz decade).	NLT 1.0 V dc and NMT 2.0 V dc at any frequency control setting.	Adjust L7 so that all settings fall into the 1.0- to 2.0-V dc reading.
	g. If decade installed in 100-Hz slot (A18), set FREQUENCY KHZ control on front panel to 09999.00 (or 09999.0). If decade installed in 10-Hz slot, set FREQUENCY KHZ control on front panel to 09999.90.		
	h. Using a frequency counter, measure the high reference input between P1-14 and P1-4 (ground).	600 ±0.5 kHz.	Check unit 10-Hz decade or end decade.
	i. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	600 ±0.5 kHz.	Check U11, U12, U13, and associated circuits.
	j. If decade installed in 100-Hz slot (A18), set FREQUENCY KHZ control on front panel to 09999.90 (or 09999.9). If decade installed in 10-Hz slot (A18), set FREQUENCY KHZ control on front panel to 09999.99.		
	k. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	510 ±0.5 kHz.	Check U11, U12, U13, and associated circuits.
	l. Measure the dc voltage at P1-12 to ground.	NLT +3.5 V dc. **Note** RCV FAULT, EXCTR FAULT, or R/E FAULT indicator lighting indicates that result of step m is satisfactory.	Check U3, U8, U9, and U10.
(Cont)	m. Ground P1-5 while noting the voltage at P1-12.	NMT 0.5 V dc.	Check U6, U7, U8, U9, and U10.

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	n. Remove P1-5 ground.		
	o. Set front-panel PWR switch off.		
	p. If testing decade installed in 100-Hz slot (A18), remove decade in 10-Hz (A17) slot from unit under test. If testing decade installed in 10-Hz slot (A17), remove end decade from unit under test.		
	q. Set front-panel PWR switch on.		
	r. Measure the dc voltage at P1-12 to ground.	NMT 0.5 V dc.	Check U1, U2, U3, and U10.
	s. Set front-panel PWR switch off.		
	t. Replace decade that was removed in step p.		

The following chart is shown with an input frequency of 600 ±5 kHz. The actual output frequency with any input frequency can be determined using the following formula.

$$AF = LF - 10\ kHz + \frac{600\ kHz - IF}{10}.$$

AF = actual output frequency at P1-1.

LF = output frequency listed in chart for associated 100- or 10-Hz frequency digit.

IF = actual input frequency.

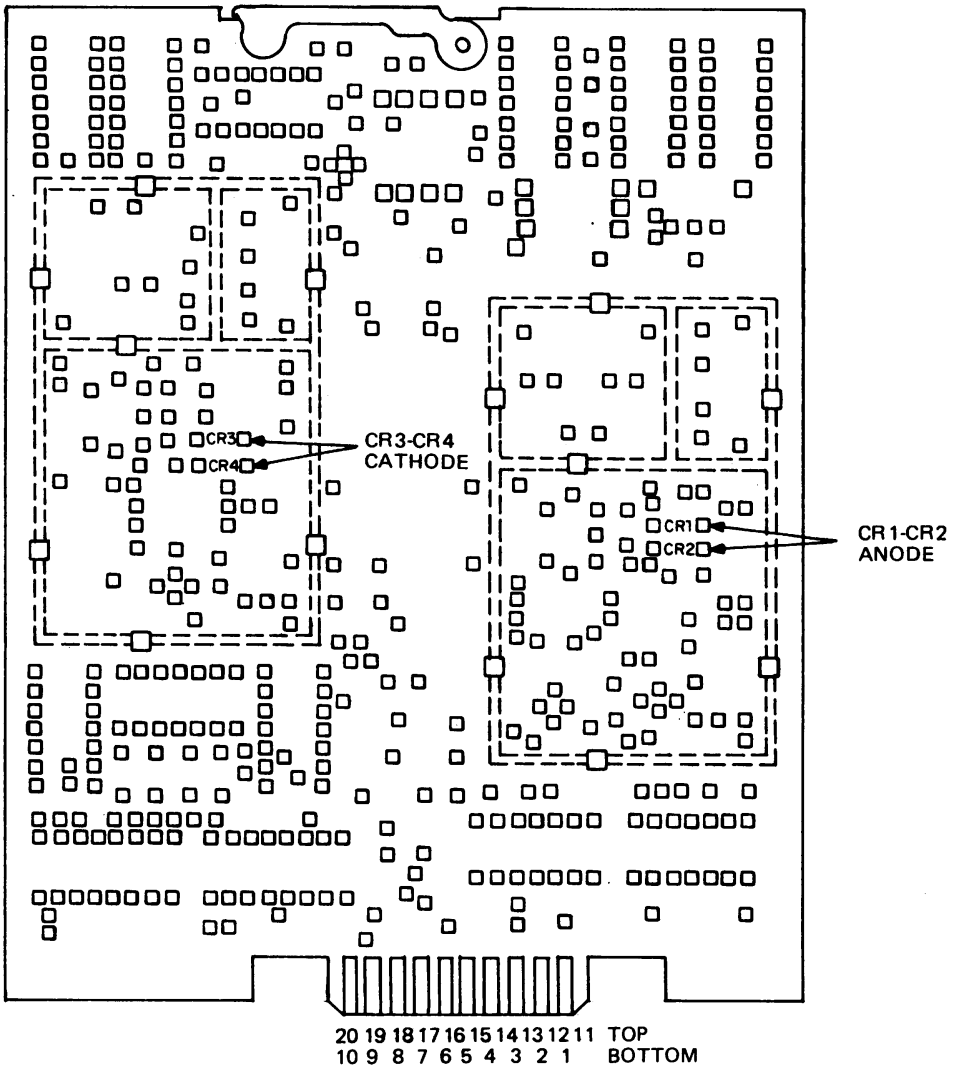
*100/10-Hz FREQ DIGIT	CR3-CR4 DC VOLTAGE	FREQ OUTPUT P1-1 (kHz)
9	10.0 ±0.1	510 ±0.5
8	**10.5	520 ±0.5
7	**11.0	530 ±0.5
6	**11.5	540 ±0.5
5	**12.0	550 ±0.5
4	**12.5	560 ±0.5
3	**13.0	570 ±0.5
2	**13.5	580 ±0.5
1	**14.0	590 ±0.5
0	**14.5	600 ±0.5

*If decade installed in 100-Hz (A18) slot, 100-Hz frequency digit position. If decade installed in 10-Hz (A17) slot, 10-Hz frequency digit position.

**Reference voltage only. Voltages will vary from board to board.

Note

Table shown with an input frequency of 600 ±5 kHz.



TP5-3056-011

Synthesizer Decade, Rear View
Figure 13

4. ALIGNMENT/ADJUSTMENT

4.1 L7 and L9 Selection, and Decade Strapping

Note

L7 and L9 can be replaced only by removing the metal cans that cover them. In emergency repairs L7, L9, and strapping can be changed on any synthesizer decade 623-2080-( ) to make the required decade (100 kHz, 10 kHz, 1 kHz, or 100/10 Hz). When L7, L9, and straps are installed as follows, the indicated decade is constructed. Testing and adjustments must be made to ensure proper operation.

4.1.1 100-kHz Decade 623-2080-001

a. Install L7, 6.75 to 11.25 μH, (242-0441-030).
b. Install L9, 6.75 to 11.25 μH, (242-0441-030).
c. Strap A to 1 and B to 2.

4.1.2 10-kHz Decade 623-2080-002

a. Install L7, 6.75 to 11.25 μH, (242-0441-030).
b. Install L9, 12.0 to 18.0 μH, (242-0441-040).
c. Strap B to 2 and C to 1.

4.1.3 1-kHz Decade 623-2080-003

a. Install L7, 12.0 to 18.0 μH, (242-0441-040).
b. Install L9, 20.8 to 31.2 μH, (242-0441-050).
c. Strap B to 2 and 1 to 2.

4.1.4 100/10-Hz Decade 623-2080-004

a. Install L7, 20.8 to 31.2 μH, (242-0441-050).
b. Install L9, 20.8 to 31.2 μH, (242-0441-050).
c. Strap B to 2 and 1 to 2.

4.2 Adjustment of L7 and L9

Note

If either L7 or L9 is replaced, both must be adjusted. Metal can shields must be installed before making these adjustments.

Refer to table 8. Perform the test procedures applicable to the associated decade.

a. For L7 and L9 adjustment in 100-kHz decade, perform test 2, steps a through d.
b. For L7 and L9 adjustment in 10-kHz decade, perform test 3, steps a through d.
c. For L7 and L9 adjustment in 1-kHz decade, perform test 4, steps a through d.
d. For L7 and L9 adjustment in 100/10-Hz decade, perform test 5, steps a through d.

5. REPAIR

Repair of the synthesizer decade is accomplished using the standard planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

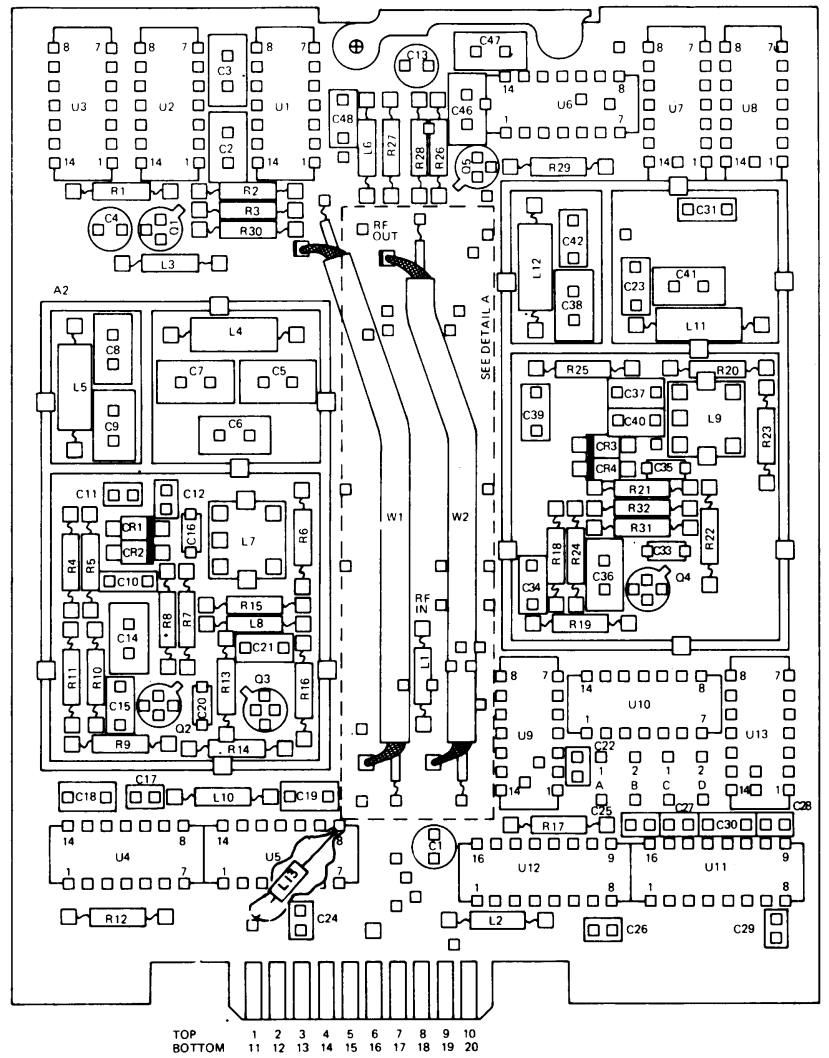
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figure 14). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

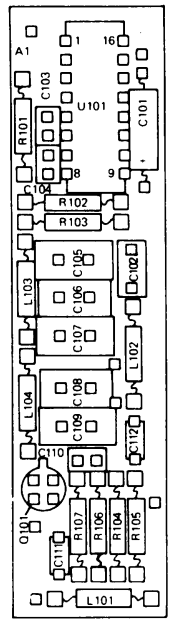
Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
100-kHz synthesizer decade	623-2080-001	REV E
10-kHz synthesizer decade	623-2080-002	REV E
1-kHz synthesizer decade	623-2080-003	REV E
100/10-Hz synthesizer decade	623-2080-004	REV E
Decade circuit card	635-0650-001	REV K
Mixer if board	635-0651-001	REV A





DETAIL A

TP5 1065-019

P/O A2 DECADE CIRCUIT CARD
(635-0650-001)

HIGH REF IN

HIGH REF GND

P/O P1

+5 V DC

+20 V DC

U1A U1B U2A U2B U2C U2D U3A U3B

Q1 2N2369A

Q2 2N918

Q3 2N918

3N187 Q101

U4A U4B U5

CR1 MV109

CR2 MV109

L7 4

U101A U101B U101C

OUTPUT

OUTPUT GND

A1 MXR IF BOARD
(635-0651-001)

635-0429 SH 1

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, AND CAPACITANCE VALUES ARE IN PICOFARADS.
2. LIGHT DASHED LINES INDICATE METAL PARTITIONED ENCLOSURES ON PC BOARD.
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.

POWER AND GROUND CONNECTIONS

U NO.	TYPE	PWR (V DC)	
		+5	GND
U1,U3,U6, U8,U13	SN74LS74N	14	7
U2,U4,U7, U9	N74LS00N	14	7
U5	SN74LS90N	5	10
U10	N74LS20N	14	7
U11,U12	SN74LS190N	16	8
U101	F4049BPC	1	8

Synthesizer Decade, Schematic Diagram
Figure 14 (Sheet 1 of 3)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	SYNTH 100-kHz DECADE 623-2080-001		A
	SYNTH 10-kHZ DECADE 623-2080-002		B
	SYNTH 1-kHZ DECADE 623-2080-003		C
	SYNTH 100/10-Hz DECADE 623-2080-004		D
A1	MIXER/IF BOARD	635-0651-001	
A2	DECADE BOARD	635-0650-001	
L1-L6	NOT USED		
L7	COIL, RF, VAR, 6.75-11.25μH	242-0441-030	A,B
L7	COIL, RF, VAR, 12-18μH	242-0441-040	C
L7	COIL, RF, VAR, 20.8-31.2μH	242-0441-050	D
L8	NOT USED		
L9	COIL, RF, VAR, 6.75-11.25μH	242-0441-030	A
L9	COIL, RF, VAR, 12-18μH	242-0441-040	B
L9	COIL, RF, VAR, 20.8-31.2μH	242-0441-050	C,D
	MIXER/IF BOARD A1 635-0651-001		
C101	CAPACITOR, FXD, ELCTLT, 6.8μF, 10%, 6V	184-9086-020	
C102	CAPACITOR, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C103,C104	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C105	CAPACITOR, FXD, MICA DIEL, 330pF, 5%, 100V	912-3915-000	
C106	CAPACITOR, FXD, MICA DIEL, 24pF, 5%, 500V	912-3843-000	
C107	CAPACITOR, FXD, MICA DIEL, 300pF, 5%, 300V	912-3912-000	
C108	CAPACITOR, FXD, MICA DIEL, 10pF, 0.5pF, 500V	912-3837-000	
C109	CAPACITOR, FXD, MICA DIEL, 220pF, 5%, 500V	912-3903-000	
C110	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C111,C112	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
L101-L104	COIL, RF, 100μH	240-2047-000	
Q101	TRANSISTOR, 3N187	352-1093-010	
R101,R102	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R103	RESISTOR, FXD, CMPSN, 1KΩ, 10%, 1/4W	745-0749-000	
R104	RESISTOR, FXD, CMPSN, 180Ω, 10%, 1/4W	745-0722-000	
R105	RESISTOR, FXD, CMPSN, 10KΩ, 10%, 1/4W	745-0785-000	
R106	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R107	RESISTOR, FXD, CMPSN, 470Ω, 10%, 1/4W	745-0737-000	
U101	INTEGRATED CKT, F4049BPC	351-8159-210	
	DECADE BOARD A2 635-0650-001		
CR1-CR4	SEMICOND DEVICE, MV109	922-6124-040	
C1	CAPACITOR, FXD, ELCTLT, 68μF, 20%, 6V	184-9102-040	
C2, C3	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 500V	912-3879-000	
C4	CAPACITOR, FXD, ELCTLT, 68μF, 20%, 6V	184-9102-040	
C5	CAPACITOR, FXD, MICA DIEL, 180pF, 5%, 500V	912-3897-000	
C6	CAPACITOR, FXD, MICA DIEL, 20pF, 5%, 500V	912-3841-000	
C7	CAPACITOR, FXD, MICA DIEL, 220pF, 5%, 500V	912-3903-000	
C8	CAPACITOR, FXD, MICA DIEL, 56pF, 5%, 500V	912-3861-000	
C9	CAPACITOR, FXD, MICA DIEL, 150pF, 5%, 500V	912-3891-000	
C10	CAPACITOR, FXD, CER DIEL, 0.039μF, 10%, 100V	913-5019-390	
C11,C12	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C13	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C14	CAPACITOR, FXD, MICA DIEL, 47pF, 5%, 500V	912-3856-000	
C15	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C16	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C17	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C18,C19	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C20	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C21	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C22	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C23	CAPACITOR, FXD, CER DIEL, 0.0027μF, 5%, 100V	913-3117-130	
C24-C29	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C30,C31	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C32	NOT USED		
C33	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C34	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C35	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C36	CAPACITOR, FXD, MICA DIEL, 47pF, 5%, 500V	912-3856-000	
C37	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C38	CAPACITOR, FXD, MICA DIEL, 43pF, 5%, 500V	912-3854-000	
C39	CAPACITOR, FXD, CER DIEL, 3300pF, 10%, 100V	913-3281-170	

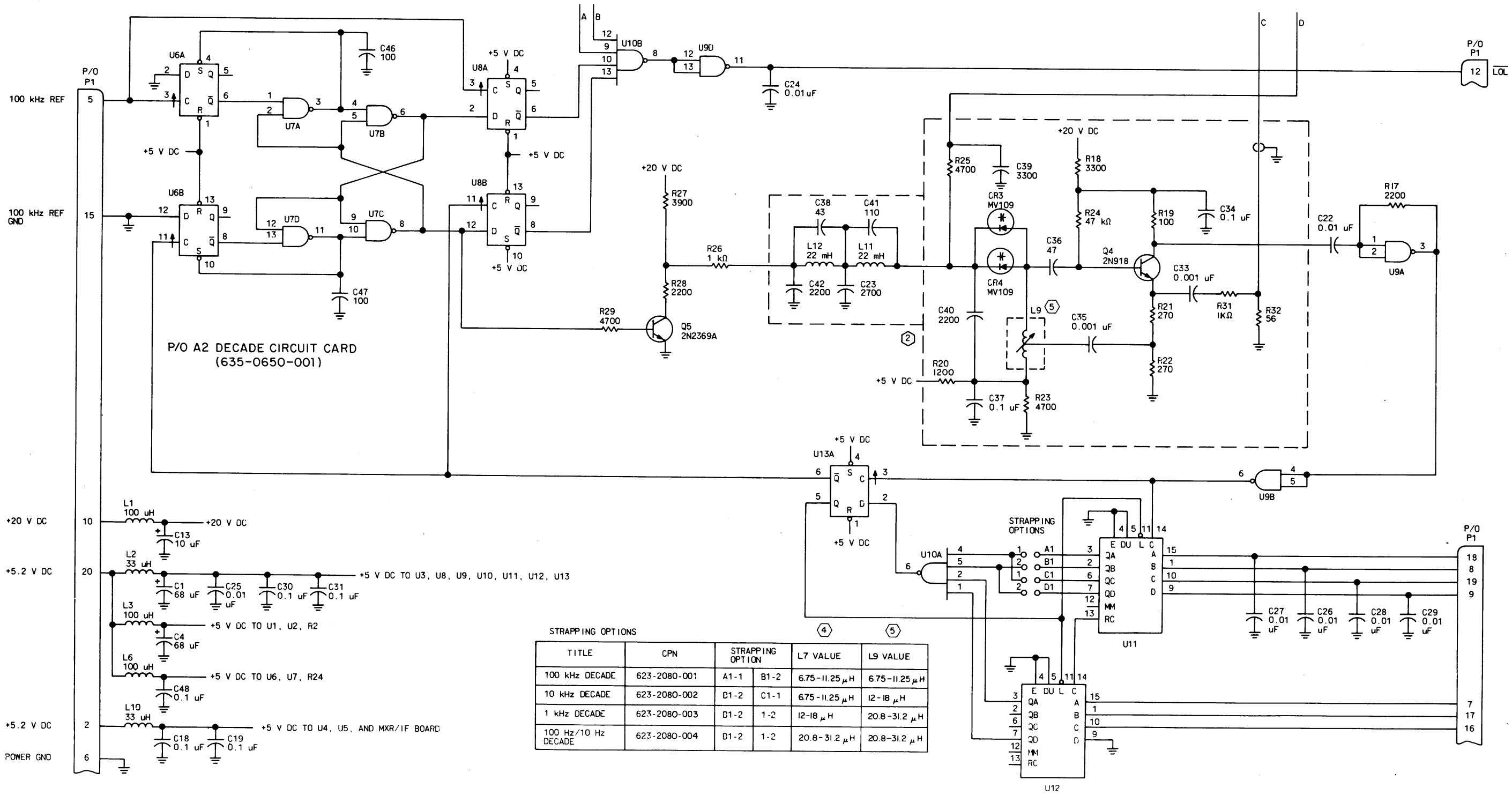
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART	USABLE ON CODE
C40	CAPACITOR, FXD, CER DIEL, 2200pF, 10%, 100V	913-3281-160	
C41	CAPACITOR, FXD, MICA DIEL, 110pF, 5%, 500V	912-3882-000	
C42	CAPACITOR, FXD, CER DIEL, 2200pF, 10%, 100V	913-3281-160	
C43-C45	NOT USED		
C46,C47	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 500V	912-3879-000	
C48	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
L1	COIL, RF, 100μH	240-2047-000	
L2	COIL, RF, 33μH	240-2041-000	
L3	COIL, RF, 100μH	240-2047-000	
L4	COIL, RF, 2200μH	240-2715-530	
L5	COIL, RF, 1800μH	240-2715-520	
L6	COIL, RF, 100μH	240-2047-000	
L7	NOT USED		
L8	COIL, RF, 100μH	240-2047-000	
L9	NOT USED		
L10	COIL, RF, 33μH	240-2041-000	
L11,L12	COIL, RF, 22,000μH	240-2715-650	
L13	COIL, RF, 1.5μH (A1)	240-2025-000	
Q1	TRANSISTOR, 2N2369A	352-0596-030	
Q2-Q4	TRANSISTOR, 2N918	352-0440-000	
Q5	TRANSISTOR, 2N2369A	352-0596-030	
R1	RESISTOR, FXD, CMPSN, 4.7KΩ, 10%, 1/4W	745-0773-000	
R2	RESISTOR, FXD, CMPSN, 1KΩ, 10%, 1/4W	745-0749-000	
R3	RESISTOR, FXD, CMPSN, 1.5KΩ, 10%, 1/4W	745-0755-000	
R4	RESISTOR, FXD, FILM, 4.22KΩ, 1%, 1/8W	705-1026-000	
R5	RESISTOR, FXD, FILM, 715Ω, 1%, 1/8W	705-0989-000	
R6	RESISTOR, FXD, CMPSN, 10KΩ, 10%, 1/4W	745-0785-000	
R7,R8	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/4W	745-0728-000	
R9	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R10	RESISTOR, FXD, CMPSN, 47KΩ, 10%, 1/4W	745-0809-000	
R11	RESISTOR, FXD, CMPSN, 3.3KΩ, 10%, 1/4W	745-0767-000	
R12	RESISTOR, FXD, CMPSN, 2.2KΩ, 10%, 1/4W	745-0761-000	
R13	RESISTOR, FXD, CMPSN, 12KΩ, 10%, 1/4W	745-0788-000	
R14	RESISTOR, FXD, CMPSN, 4.7KΩ, 10%, 1/4W	745-0773-000	
R15	RESISTOR, FXD, CMPSN, 2.2KΩ, 10%, 1/4W	745-0761-000	
R16	RESISTOR, FXD, CMPSN, 470Ω, 10%, 1/4W	745-0737-000	
R17	RESISTOR, FXD, CMPSN, 2.2KΩ, 10%, 1/4W	745-0761-000	
R18	RESISTOR, FXD, CMPSN, 3.3KΩ, 10%, 1/4W	745-0767-000	
R19	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R20	RESISTOR, FXD, CMPSN, 1.2KΩ, 10%, 1/4W	745-0752-000	
R21,R22	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/4W	745-0728-000	
R23	RESISTOR, FXD, CMPSN, 4.7KΩ, 10%, 1/4W	745-0773-000	
R24	RESISTOR, FXD, CMPSN, 47KΩ, 10%, 1/4W	745-0809-000	
R25	RESISTOR, FXD, CMPSN, 4.7KΩ, 10%, 1/4W	745-0773-000	
R26	RESISTOR, FXD, CMPSN, 1KΩ, 10%, 1/4W	745-0749-000	
R27	RESISTOR, FXD, CMPSN, 3.9KΩ, 10%, 1/4W	745-0770-000	
R28	RESISTOR, FXD, CMPSN, 2.2KΩ, 10%, 1/4W	745-0761-000	
R29	RESISTOR, FXD, CMPSN, 4.7KΩ, 10%, 1/4W	745-0773-000	
R30	RESISTOR, FXD, CMPSN, 3.9KΩ, 10%, 1/4W	745-0770-000	
R31	RESISTOR, FXD, CMPSN, 1KΩ, 10%, 1/4W	745-0749-000	
R32	RESISTOR, FXD, CMPSN, 56Ω, 10%, 1/4W	745-0704-000	
U1	INTEGRATED CKT, SN74LS74N	351-1525-040	
U2	INTEGRATED CKT, N74LS00N	351-1523-110	
U3	INTEGRATED CKT, SN74LS74N	351-1525-040	
U4	INTEGRATED CKT, N74LS00N	351-1523-110	
U5	INTEGRATED CKT, SN74LS90N	351-1636-010	
U6	INTEGRATED CKT, SN74LS74N	351-1525-040	
U7	INTEGRATED CKT, N74LS00N	351-1523-110	
U8	INTEGRATED CKT, SN74LS74N	351-1525-040	
U9	INTEGRATED CKT, N74LS00N	351-1523-110	
U10	INTEGRATED CKT, N74LS20N	351-1523-130	
U11,U12	INTEGRATED CKT, SN74LS190N	351-1527-040	
U13	INTEGRATED CKT, SN74LS74N	351-1525-040	

MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Added A2L13, 1.5μH	635-0650-001 REV K and above

Synthesizer Decade, Schematic Diagram
Figure 14 (Sheet 2)



STRAPPING OPTIONS

TITLE	CPN	STRAPPING OPTION		L7 VALUE	L9 VALUE
100 kHz DECADE	623-2080-001	A1-1	B1-2	6.75-11.25 μH	6.75-11.25 μH
10 kHz DECADE	623-2080-002	B1-2	C1-1	6.75-11.25 μH	12-18 μH
1 kHz DECADE	623-2080-003	B1-2	1-2	12-18 μH	20.8-31.2 μH
100 Hz/10 Hz DECADE	623-2080-004	B1-2	1-2	20.8-31.2 μH	20.8-31.2 μH

Synthesizer Decade, Schematic Diagram
Figure 14 (Sheet 3)